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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,140	02/17/2004	William E. Dougherty JR.	YOR920030437US1 (8728-653)	9678
46069	7590	11/20/2006	EXAMINER DINH, PAUL	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			ART UNIT 2825	
			PAPER NUMBER	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/780,140	Applicant(s) DOUGHERTY ET AL.	
	Examiner Paul Dinh	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

This is a response to the pre-appeal brief request filed on 10/27/06.

The previous rejections and allowability have been withdrawn in view of the pre-appeal brief request.

New grounds of rejections have been cited in this office action in view of the pre-appeal brief request.

Claims 1-14 are pending.

Claim Objections

Claim 3 is objected to because the limitation “wherein creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design comprises creating a structural metric prior to physical design” is redundant.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain patent therefor, subject to the conditions and requirements of this title.

Claims 1-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subjected matter.

MPEP 2106 [R-5], section II, subsection A outlines: “The claimed invention as a whole must be useful and accomplish a practical application. That is, it must produce a “useful, concrete and tangible result.” State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02”.

Claim 1, 13-14 and dependencies of claim 1 are rejected because a useful/tangible/practical/concrete result/application/improvement/effect/advantage is not recited in claim 1, 13-14 (Slash = and/or).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

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The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1, 13-14 (and dependencies of claim 1) are rejected because the limitation “the structural metric being proportional to a routability of the circuit design model after the physical design” finds no clear support in the disclosure.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 13-14 are rejected because “prior to a physical design” in claims 1 and 13-14 is unclear and incomplete as to physical design of what.

Claims 1 and 13-14 are rejected because “structural metric” is not defined in claims 1 and 13-14. Thus make the claim unclear and thus indefinite because. It is not clear what “structural metric” means to encompass. What does “structural metric” represents; the applicants argue in the pre-appeal brief request that “structural metric” is a measure. This is an incomplete, vague, ambiguous answer; i.e., measure of what or measured in terms of what.

Claims 1 and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps/elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

Claims 1, 13-14 recite: “the structural metric being proportional to a routability of the circuit design model after the physical design”. As the claims present, what step/functions/elements in the claim that make the structural metric being proportional to a routability of the circuit design model after the physical design”. The applicants argue in the pre-appeal brief request that “structural metric” is a measure. This is an incomplete, vague, ambiguous answer; i.e., a measure of what or measured in terms of what that make the measure proportional to a routability of the circuit design model after the physical design”

Claims 1 and 13-14 are rejected 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claims 1, 13-14 recite: “Creating a structural metric prior to physical design, the structural metric being proportional to a routability of the circuit design model after the physical design”. As the claim present, what structural cooperative relationships to allow/ensure the structural metric being proportional to a routability of the circuit design model after the physical design. The applicants argue in the pre-appeal brief request that “structural metric” is a measure. This is an incomplete, vague, ambiguous answer; i.e., a measure of what or measured in terms of what that make the measure proportional to a routability of the circuit design model after the physical design”

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Gupta et al (US Pub. 2004/0068711)

(Claim 1 and similarly recited claims 13-14)

Creating a structural metric prior to physical design

(Structural metric is, one or more of: i.e., a measure/consideration of routability/timing convergence (any one of field of invention, summary, para 0008), forming of architecture designs (para 0009, 0021), architecture representation (para 0010), cost (para 0021, 0035), representation/instantiation that will possibly result in unacceptable interconnect delay or congestion (any one of abstract, summary, para 0040), interconnect routability, routing congestion (para 0040-0043) routing congestion (para 0042, 0063), distance or delay (fig 2), netlist that is more amenable to physical design (para 0063), measure/estimation in terms of cost/silicon area/number of components/wires (para 0003); hardware structure (fig 6-7), cost estimate in terms of placements (para 0035); probability of a model (para 0048); empirical calibration (para 0048); the ratio of circuits (para 0048), measuring the amount of average slack at various design points (para 0048), estimation of routing congestion (para 0049); hardware spec generation (para 0095); cost and performance (para 0096), insofar structural metric is best understood.

Structural metric prior to physical design disclosed in one or more of: i.e., para 0009, 0021 (architecture designs that are better suited for subsequent physical synthesis, routability considered before physical synthesis), para 0048 (the model determines the probability "p" of successful synthesis design (e.g., one-pass timing convergence and routing), para 0048 (empirical calibration methodology may be used to estimate such physical synthesis), para 0048 (the ratio of circuits that successfully pass the physical design), para 0095 (hardware Specification is then ready for physical synthesis) para 0096 (timing convergence and routability (besides meeting additional design objectives such as cost and performance) during subsequent physical synthesis))

The structural metric being proportional to a routability of the circuit design model after the physical design; and

(As best understood, this limitation is fairly/equivalently disclosed/ performed in/by one or more of the followings:

1. Para 0003, "the cost of a circuit is typically measured in terms of its silicon area and may be estimated from the number of components (wires)";
2. Para 0008-0009, "routability considerations are taken into account during architecture synthesis so as to reduce the need for manual corrective action during physical synthesis", "cost-effective due to improved utilization of clock periods and improved routability of interconnects among hardware elements";
3. Para 0043, "predicts which dependencies in the code will affect routing delay and/or congestion in the hardware", and
4. Para 0048-0049, "estimate such physical synthesis metrics during architectural synthesis, estimate of the routing congestion and the necessary slack in order to meet timing",

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“empirical calibration methodology may be used to estimate such physical synthesis metrics during architectural synthesis”

5. *Para 0063, “the netlist leads to fewer long wires and/or less routing congestion during physical design thereby improving routability in comparison to existing techniques.*

6. *Para 0096, “By virtue of this invention, the hardware circuit would be likely to have one-pass timing convergence and routability (besides meeting additional design objectives such as cost and performance) during subsequent physical synthesis. After physical synthesis, the result for an FPGA-target ...”*

7. *Para 0096, “timing convergence and routability (besides meeting design objective such as cost and performance) during subsequent physical synthesis. After physical synthesis, the result for an FPGA-target...”*

Note that although the terms “proportional” is not used in the prior art, the above mentioned items 1-7 *fairly/equivalently disclose the limitation* “The structural metric being proportional to a routability of the circuit design model after the physical design” insofar the limitation is understood)

Using the structural metric during logic synthesis to create an optimized circuit design model (one or more of title, abstract, field of invention, para 0005, 0008, 0009, 0021, 0023).

(Claim 2) wherein using the structural metric during logic synthesis to create an optimized circuit design model comprises adding, deleting or substituting one or more circuits using a combination of Boolean, algebraic and electrical optimizations to create an optimized circuit design model (fig 1-3).

(Claim 3) wherein creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design comprises creating a structural metric prior to physical design (see above rejection of claim 1 for this redundancy), the structural metric when applied to a graph of the circuit design model (one or more of: fig 3, para 0024, 0028, 0032-0033, 0035, 0037, 0040, 0043, 0045, 0047, 0051, 0054, 0058, 0065, 0070, 0075, 0076, 0082, 0084, 0088) is directly proportional to a routing congestion of the circuit design model after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design model (one or more of: para. 0040-0043, 0057, 0062-0063, 0092)

(Claims 4-5) wherein using the structural metric during logic synthesis comprises using the structural metric during a technology independent synthesis stage of the logic synthesis (one

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or more of para 0002, 0021, 0061-0062, 0096); during the technology mapping stage of the logic synthesis (one or more of para 0002, 0021, 0061-0062, 0096).

(Claim 6) wherein using the structural metric during logic synthesis comprises using the structural metric during a buffering stage of the logic synthesis (para 0060, 0072)

(Claim 7) further comprising incrementally updating the structural metric when logic changes are made to the circuit design model (one or more of fig 1-3, 6-8, para 0034, 0043-0044, 0056, 0058, 0079-0081).

(Claim 8) wherein incrementally updating the structural metric logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary (one or more of fig 1-3, 6-8, para 0034, 0043-0044, 0056, 0058, 0079-0081).

(Claim 9) wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073).

(Claim 10) wherein creating the structural metric comprises creating any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), expansion metric (one ore more of para 0024, 0033, 0050-0054)

(Claim 11) wherein creating a structural metric comprises: generating one or more possible optimizations (this invention about generating one or more possible optimizations i.e., cost, components, power, area, delay, reduction/minimizing manual work, cut, net, congestion, hardware, distance, wire lengths, etc.); incrementally updating the structural metric when the optimizations are made to the circuit design model to evaluate the cost of applying each of the one or more possible optimizations to the circuit design model (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073), the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric (one ore more of para 0024, 0033, 0050-0054); evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073); selecting an optimization from the one or more possible optimizations with the lowest structural metric cost (one or more of para 0035, 0037,

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0039, 0046-0047, 0055, 0072-0073); and applying the optimization to the circuit design model (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073),.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh

Primary Examiner

A handwritten signature in black ink that reads "Paul Dinh". The signature is written in a cursive style with a long, sweeping underline that extends to the right.